



# **A Reconfigurable Parallel Pipelining VLSI Architecture for Low Latency 3-D Dwt Lifting**

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**ABSTRACT:** Optimizing image compression is a craft balance between compression and PSNR ratio. Numerous 2D wavelet mechanisms are introduced throughout the literature and reached its superiority over various other compression schemes. This paper work presents a novel methodology of 3D wavelet for lifting for video and color band compression, in this method the spatial and frequency relation between video frames will be considered for achieving better compression and reconstruction PSNR ratios. A parallel processing VLSI architecture is demanded due to the implications of complex and delay inducing equations, whereas the design constraint of a VLSI parallel architecture required to have a fixed number of picture groups for processing i.e. for  $j^{\text{th}}$  level of the video frame,  $j$  number of processing units are required to operate in parallel. This work proposes to optimize this limitation by designing a dynamically reconfigurable 3D wavelet lifting architecture.

**KEYWORDS:** Wavelet, Lifting Scheme, VLSI, FPGA

## **I. INTRODUCTION**

High Quality Image compression schemes are in demand due to the vast increment in Visual database. Wavelet lifting is one of a literature favorite mechanism for simple and effective image compression. 2-D Image compression methodologies have reached to an extreme in Peak SNR and Mean Square Error achievement. 3-D Image or Video compression techniques need to be refined from complex motion estimation to simple wavelet scheme.

## **II. 2-D IMAGE COMPRESSION**

Image compression leads image file size reduction in order to include them as attachments in emails, among other uses. Best image compression should consider the balance between PSNR and compression ratio. High-resolution images are too large to work with in their full size, and so compression algorithms are required (JPEG, PNG, TIF). Wavelet lifting is one of the best and effective image compression technique for high compression and PSNR ratio.

### **A. VLSI ARCHITECTURE OF 2-D WAVELET LIFTING**

The block diagram of the proposed architecture is shown in Fig. 4 for 1 level 2-D DWT. Input is provided block by block using a simple Array Function Unit (AFU).

The first stage of the pipeline consists of a low-pass and a high-pass row processor, named LPR and HPR respectively.

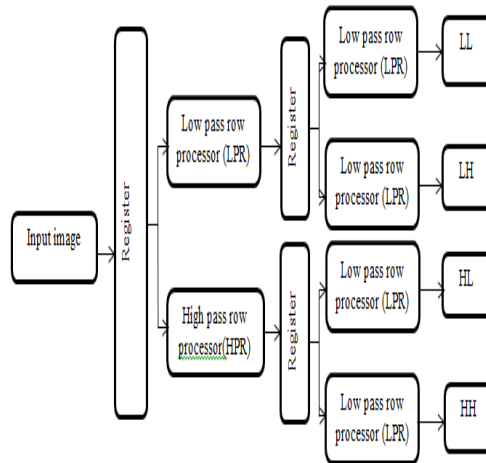
As mentioned earlier, the output of LPR and HPR are passed to the next pipeline stage consisting of two low-pass and two-high pass column processors, named LPC and HPC respectively. LPC and HPC are responsible of calculating the approximation and detail coefficients.

Note that subsampling is implicitly incorporated in the architecture and thus no components for the row or column subsampling shown in Fig. 1 are needed. Resulting from the modified image scan described in the previous section, a match between the inter-pixel distance after subsampling and the 2x2 Haar wavelet filter size, is found.

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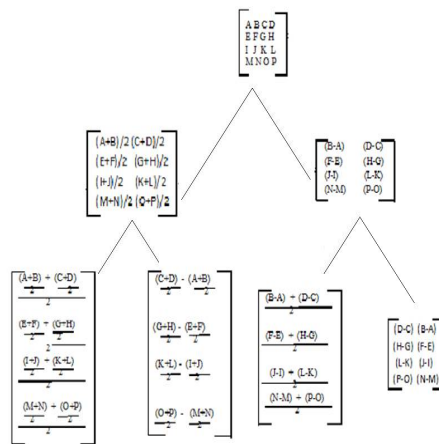


**Fig: vlsi architecture of 2-D wavelet lifting**

If the filter masks are shifted by 1 pixel each cycle, the 2x1 block, obtained in Fig. 3, is clearly redundant since it will be eliminated after subsampling. Therefore, instead of shifting the filter masks by 1 pixel each cycle, it is shifted 2 pixels, and no explicit subsampling components are required anymore.

### B.2D WAVELET LIFTING EQUATION

- The 2D image is splinted into following equations.



### C. ADVANTAGES OF 2-D

- Simple processing methods.
- Less computation time.
- Effective in linear image.

## III. 3-D WAVELET LIFTING

3-D wavelet lifting will be processed in multilevel frames like a video. 3-D wavelet video compression can be an effective substitute to video motion estimation technique. Due to the image sequence complexity, high memory and



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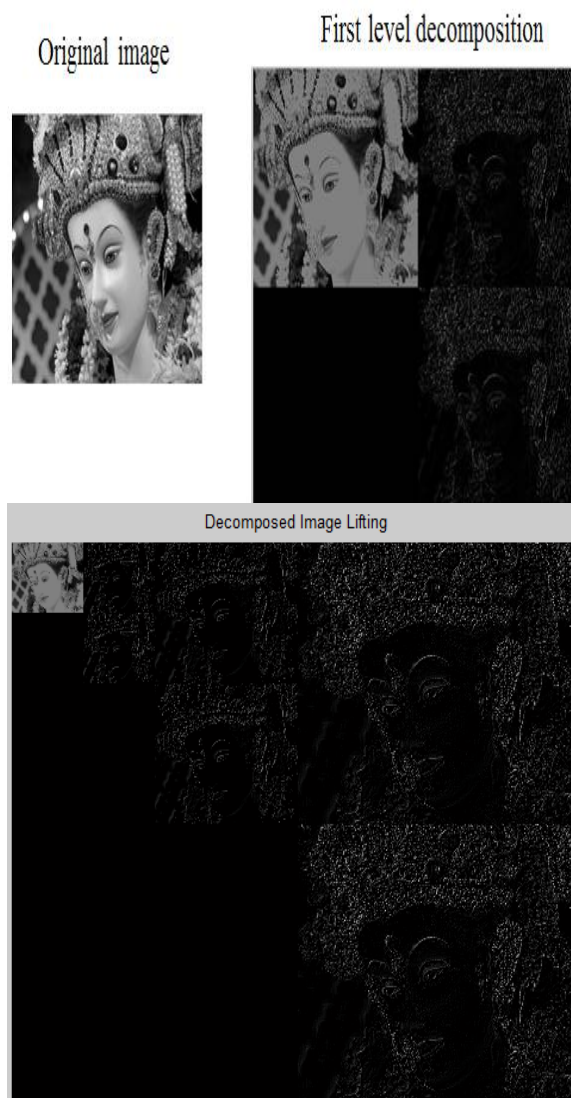
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power requirements are demanded. Parallel and pipelining VLSI architectures are required to compensate the speed and latency demerits. Color band compression involves the following approaches:

- R band (RED band).
- G band (GREEN band).
- B band (BLUE band).

## EXAMPLE



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## A. VIDEO COMPRESSION OR 3-D COMPRESSION

Video can be assumed as a 3-D image due to its frame behind the frame storage mechanism. Motion Estimation is a Complex and high cost requiring video compression method, in which the motion difference between the video frames will be stored instead of entire frame which leads better compression but difficult reconstruction.



Fig: 3D video compression

## B. 3D WAVELET VLSI ARCHITECTURE

3D like 2D wavelet VLSI architecture, but it has N number of stages. Each stage having one processing elements. First video input is given to the video frames and it is connected with image frame splitting. It splinted into number of stages i.e., 1,2,.....n. Each stage has one processing elements, this will be includes register array, predict and update. Then each processing elements gives four frequency bands.3D wavelet video compression can be an effective substitute to video motion estimation technique. Due to the image sequence complexity, high memory and power requirements are demanded. Parallel and pipelining VLSI architectures are required to compensate the speed and latency demerits

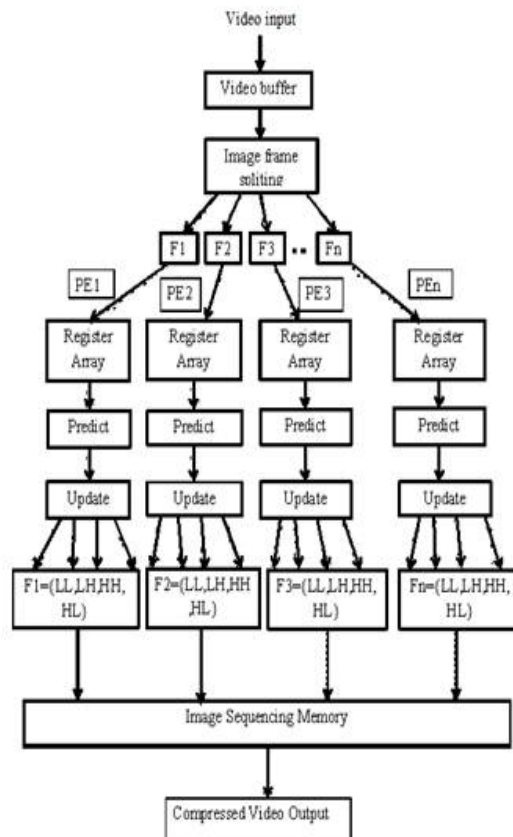


fig: 3-D wavelet VLSI architecture



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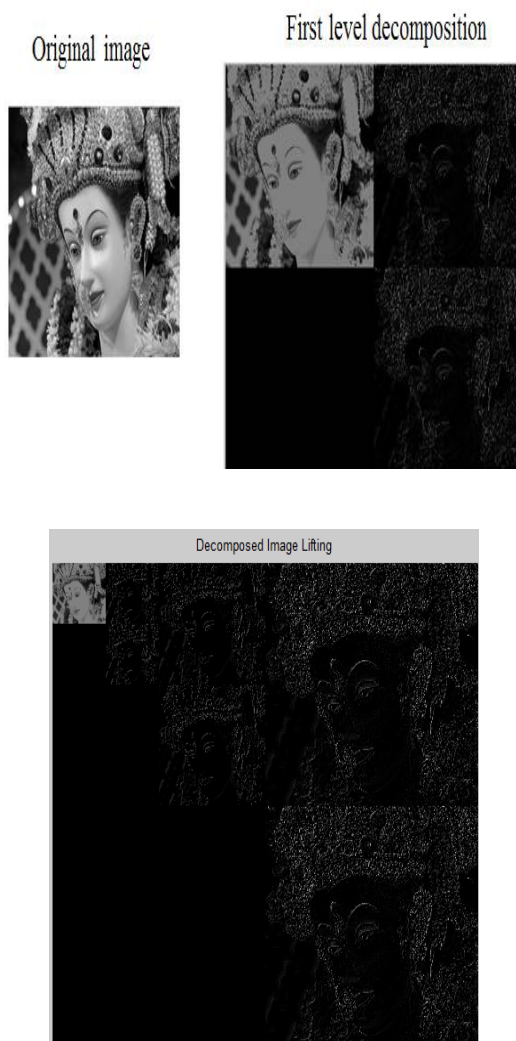
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## V. ADAPTIVE PARALLEL PIPELINING 3-D WAVELET (PROPOSED SYSTEM)

- Picture groups are not restricted.
- Ex: Fixed number of frames alone can be processed.
- Adaptive image frames can be parallel processed with in the available PE with dynamic scheduling.
- F1->predict complete F1->update and f5->prediction state ,
- f2->prediction and f2->update
- f3->Prediction, f5->Update and f3->update state.
- 

## VI. EXPERIMENTAL RESULT

### A.2\_D IMAGE COMPRESSION:





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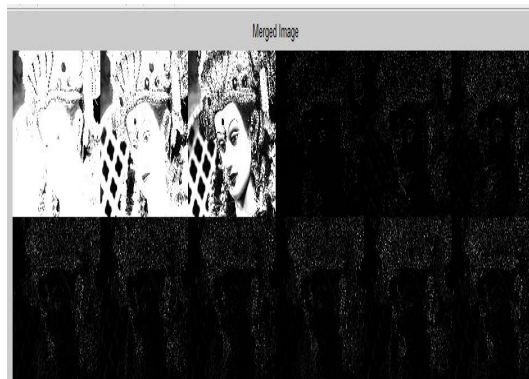
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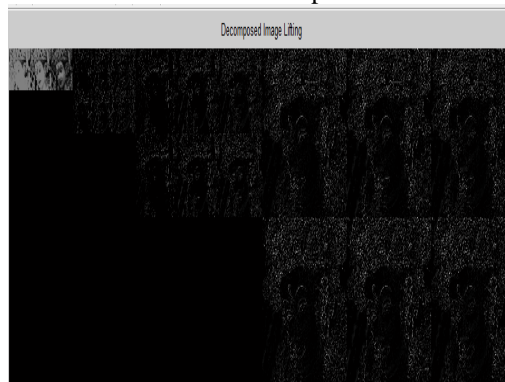
## B.3\_D IMAGE COMPRESSION:



Original image



First level decomposition



Multi level decomposition

## C.3\_D VIDEO COMPRESSION:





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## VI. CONCLUSION

The first phase of the project deals with a novel design of 2D supported and 3D supported DWT has been designed and tested using MATLAB simulation tool. The compression rate of 2D image using DWT is more than 50% and the estimation time is very low, in case of 3D DWT the execution time is comparatively high but the compression ratio is achieved more than 25%. Thus the software testing of 3D DWT is tested in 2D, 3D and video domains. The second phase of the project provides low latency by using parallel pipelining VLSI architecture.

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